AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [04] on page 2 as follows:

[04] Substrates based on "strained silicon" ~~has~~ have attracted interest as a semiconductor material which provides increased speeds of electron and hole flow therethrough, thereby permitting fabrication of semiconductor devices with higher operating speeds, enhanced performance characteristics, and lower power consumption. A very thin, tensilely strained, crystalline silicon (Si) layer is grown on a relaxed, graded composition of silicon-germanium (SiGe) buffer layer several microns thick, which SiGe buffer layer in turn is formed on a suitable crystalline substrate, e.g., a Si wafer or a silicon-on-insulator (SOI) wafer. The SiGe buffer layer typically contains 12 to 25 at.% Ge. Strained Si technology is based upon the tendency of the Si atoms, when deposited on the SiGe buffer layer, to align with the greater lattice constant (spacing) of Si and Ge atoms therein (relative to pure Si). As a consequence of the Si atoms being deposited on a substrate (SiGe) comprised of atoms which are spaced further apart, they "stretch" to align with the underlying Si and Ge atoms, thereby "stretching" or tensilely straining the deposited Si layer. Electrons and holes in such strained Si layers have greater mobility than in conventional, relaxed Si layers with smaller inter-atom spacings, i.e., there is less resistance to electron and/or hole flow. For example, electron flow in strained Si may be up to about 70% faster compared to electron flow in conventional Si. Transistors and IC devices formed with such strained Si layers can exhibit operating speeds up to about 35% faster than those of equivalent devices formed with conventional Si, without necessity for reduction in transistor size.

Please amend paragraph [16] on pages 4 and 5 as follows:

[16] The present invention addresses and solves the problem of simultaneously optimizing the drive currents for PMOS and NMOS transistors based on strained Si substrates in a cost effective, efficient manner. The present invention stems from the recognition that the hole mobility in SiGe is higher than the hole mobility in strained Si. Accordingly, embodiments of the present invention comprise strategically removing the strained Si layer from the PMOS region and forming the PMOS transistor directly on the underlying SiGe layer. Further, in accordance with the present invention, a high dielectric constant (k) material is deposited on the SiGe layer. Advantageously, by depositing a high dielectric constant (k) material as the gate dielectric layer for the PMOS transistor, the thickness of the gate dielectric layer can be increased to achieve capacitance comparable to that achieved utilizing of a lower dielectric constant (k) material at an undesirably reduced thickness. In other words, the leakage for the PMOS transistor having a thick high dielectric constant (k) gate dielectric layer would be comparable to the leakage of the NMOS transistor having a thin low k gate dielectric layer, and the ~~of~~ drive current of the PMOS transistor would be increased comparable to the of drive current to the NMOS transistor. Thus, the SiGe channel PMOS transistor in accordance with the embodiments of the present invention has a higher carrier mobility and, hence, a higher drive current than would be the case for a PMOS transistor formed on a strained Si layer.

Please amend paragraph [17] on page 5 as follows:

[17] An embodiment to the present invention is schematically illustrated in Figs. 1 through 4. Adverting to Fig. 1. STI structures 12 are formed in a substrate comprising a layer of

strained Si 11 on a layer of SiGe 10. The region at the left of Fig. 1 is designated as the PMOS region, while the region at the right is designated as the NMOS region. A thermal oxide layer 13 is then formed on strained Si layer ~~13~~ 11, in a conventional matter, as by heating in an oxygen ambient. Thermal oxide layer 13 is typically formed at a thickness of 10Å to 20Å.